Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OUTPUT A**
2. **–INPUT A**
3. **+INPUT A**
4. **GND**
5. **+INPUT B**
6. **–INPUT B**
7. **OUTPUT B**
8. **VCC**

**.036”**

**7 8 1**

**3**

**2**

**5**

**6**

**4**

**MASK**

**REF**

**358**

**S1**

**.025”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: FLOAT**

**Mask Ref: 358**

**APPROVED BY: DK DIE SIZE .025” X .036” DATE: 11/11/21**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: LM358**

**DG 10.1.2**

#### Rev B, 7/1